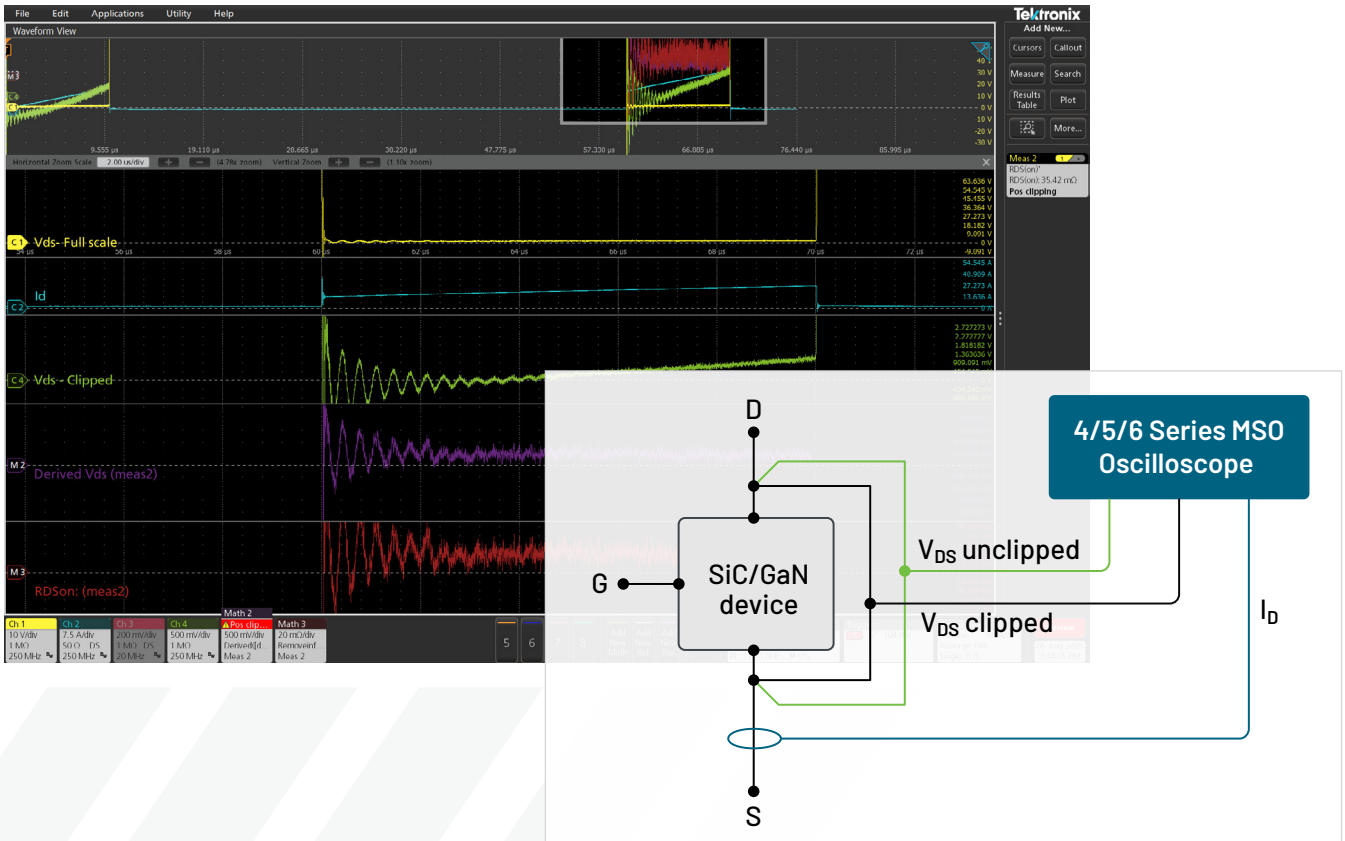
Tektronix®

Measuring Dynamic $R_{DS(on)}$ Without a Clamping Circuit

APPLICATION NOTE



Introduction

Dynamic on state resistance, $R_{DS(on)}$, is an important parameter for designers working to understand the impact of charge trapping in their power converter designs. However, the body of knowledge around measurement techniques is still relatively young. Traditional techniques for measuring dynamic $R_{DS(on)}$ rely on diode clamping circuits to allow oscilloscopes to measure drain to source voltage with adequate resolution, without overdriving the input of the scope. A new software clamping method, introduced in Tektronix Wide Bandgap Double Pulse Testing measurement software for the 4, 5 and 6 Series MSO oscilloscopes, uses a unique double-probing technique that eliminates the need for a clamping circuit.

What is Dynamic $R_{DS(on)}$?

Dynamic $R_{DS(on)}$ is the average resistance between a FET's drain and source terminals when it is turned on during switching. Drain-to-source resistance, $R_{DS(on)}$, is an important parameter for any FET since it is a key determinant of conduction loss and efficiency. $R_{DS(on)}$ is computed as the ratio of the drain-to-source Voltage (V_{DS}) and the Drain Current (I_D), and can be represented as a function of time as:

$$R_{DS(on)}(t) = \frac{V_{DS}(t)}{I_D(t)}$$

$R_{DS(on)}$ can then be represented as an average value of this function during the on portion of a switching cycle.

Dynamic $R_{DS(on)}$ occurs due to charge trapping phenomena in complex semiconductor structures. Researchers studying GaN semiconductors are especially interested in dynamic $R_{DS(on)}$. GaN FETs can experience a phenomenon known as current collapse, in which dynamic $R_{DS(on)}$ increases. This can occur when electrons become trapped within the device structure in the off state, when a high voltage is present between the drain and source. Although less critical for SiC devices, designers may also be interested in measuring dynamic $R_{DS(on)}$.

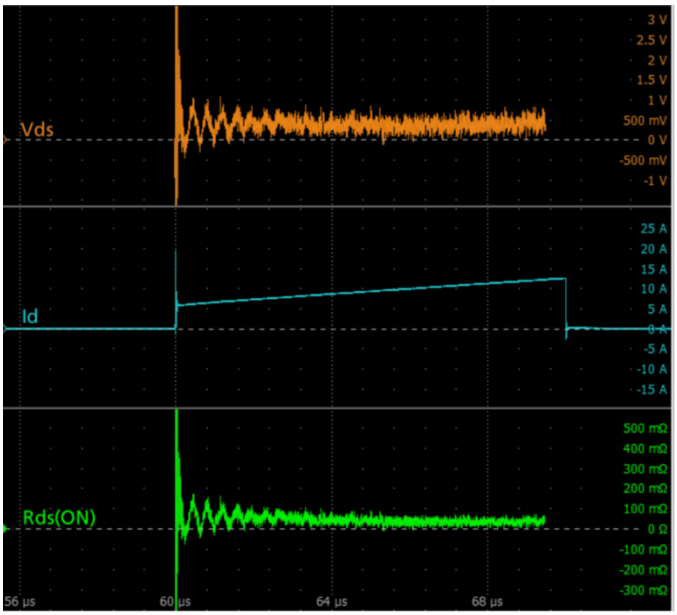


Figure 1. The $R_{DS(on)}$ waveform is the ratio of V_{DS} to I_D as they change during the on state.

Challenges in Measuring Dynamic $R_{DS(on)}$

To measure $R_{DS(on)}$, one must be able to accurately measure $V_{DS}(t)$. The main challenge in measuring $R_{DS(on)}$ arises from the need to measure a small ON voltage within a high-amplitude switching signal. The amplitude of the switching voltage, $V_{DS}(t)$, can be 800 V or more, depending on the application. However, in the on-state, $V_{DS}(t)$ will be low, on the order of 10 V or less, as shown in **Figure 2**. In addition, GaN and SiC FETs can switch with extremely high slew rates. These factors result in significant measurement challenges:

- Capturing the V_{DS} signal over its full range results in poor digital resolution for $V_{DS(on)}$. The ADC quantization error represents a large proportion of the signal. This results in large quantization noise.
- Simply increasing vertical sensitivity on the oscilloscope results in overdriving input amplifiers on the measurement system.Unless corrected, this results in measurement error during overdrive recovery.
- Fast slew rates introduce aberrations due to parasitic inductance and capacitance. These take time to settle out.

Since the switching voltage V_{DS} can be high and may be floating relative to ground, it is common to use high voltage differential probes to measure the switching voltage.

Differential probes help to avoid grounding issues which can reduce the accuracy of $R_{DS(on)}$ measurements. THDP Series differential probes are often on hand in power labs. For these reasons, THDP Series probes have been tested for use in this method and are recommended.

As noted, if one uses a low sensitivity (high V/div) to capture the entire range of V_{DS}, the voltage during the off state is acquired with low resolution since it represents just a small portion of the scope's analog-to-digital converter (ADC) and the probe's amplifier range. One possible approach is to acquire the low ON voltage at a high sensitivity (low V/div) in order to take full advantage of the differential probe and scope range. Unfortunately, acquiring a high amplitude signal with high sensitivity will overdrive the amplifier in the differential probe, causing it to produce inaccurate data during a short period of overdrive recovery.

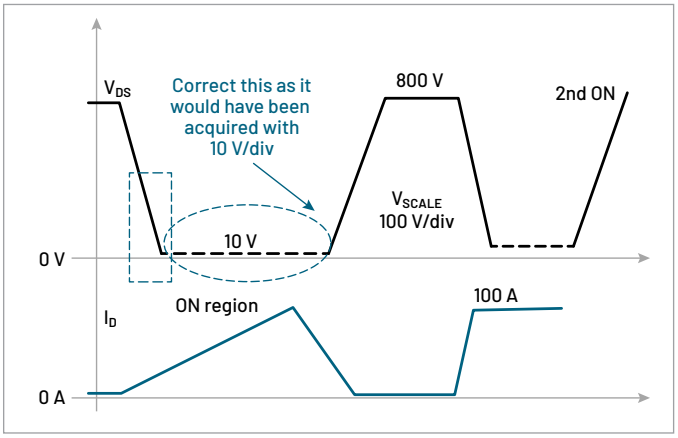


Figure 2. The high amplitude of V_{DS}, along with the small ON-state voltage, makes it challenging to measure $R_{DS(on)}$. This new method enables high sensitivity measurements with corrections.

Traditionally an external diode clamping circuit has been used to eliminate the high-voltage portion of $V_{DS}(t)$. While this approach can be effective, it has some drawbacks:

- Introduces additional parasitic capacitance, inductance and resistance into the signal path
- Introduces voltage offset associated with the RC time constant of the resistor and parasitic capacitances of diodes.
- Voltage peaks increase with value of the resistance and can be several times the clamping voltage.
- Adds additional cost to the test system

The new software clamping technique in WBT-DPT measurement automation software enables designers to make quick measurements of dynamic $R_{DS(on)}$ with equipment they may already have on hand.

A New Oscilloscope-based Approach to Clamping

Tektronix' software clamping method eliminates the need for dedicated clamping circuitry. Instead, it relies on an oscilloscope with two high voltage differential probes attached across the FET to measure drain-source voltage (V_{DS}). As shown in **Figure 3**, two instances of V_{DS} voltage are measured using two differential probes with each probe is set to a different sensitivity.

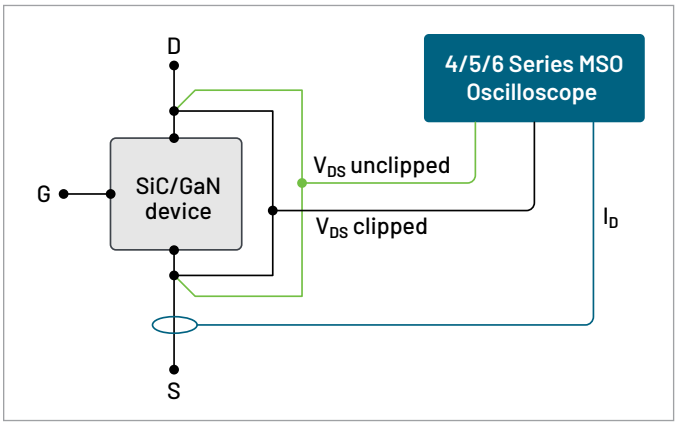


Figure 3. Two high-voltage differential probes are used to measure V_{DS}. One probe is set to a high range (e.g. 1500 V) and high vertical scale (e.g. 100 V/div). The other is set for a low range (e.g. 150 V) and lower vertical scale (e.g. 10 V/div).

- One differential probe captures the entire high to low transition on V_{DS} as the FET turns off.
- The other differential probe captures only the $R_{DS(on)}$ region at high sensitivity, providing high resolution while the FET is turned on and V_{DS} is small. This has the effect of intentionally clipping the signal on V_{DS}. Note that this method is similar to clipping the signal using a diode clamping circuit but requires the application of corrections to get good results.

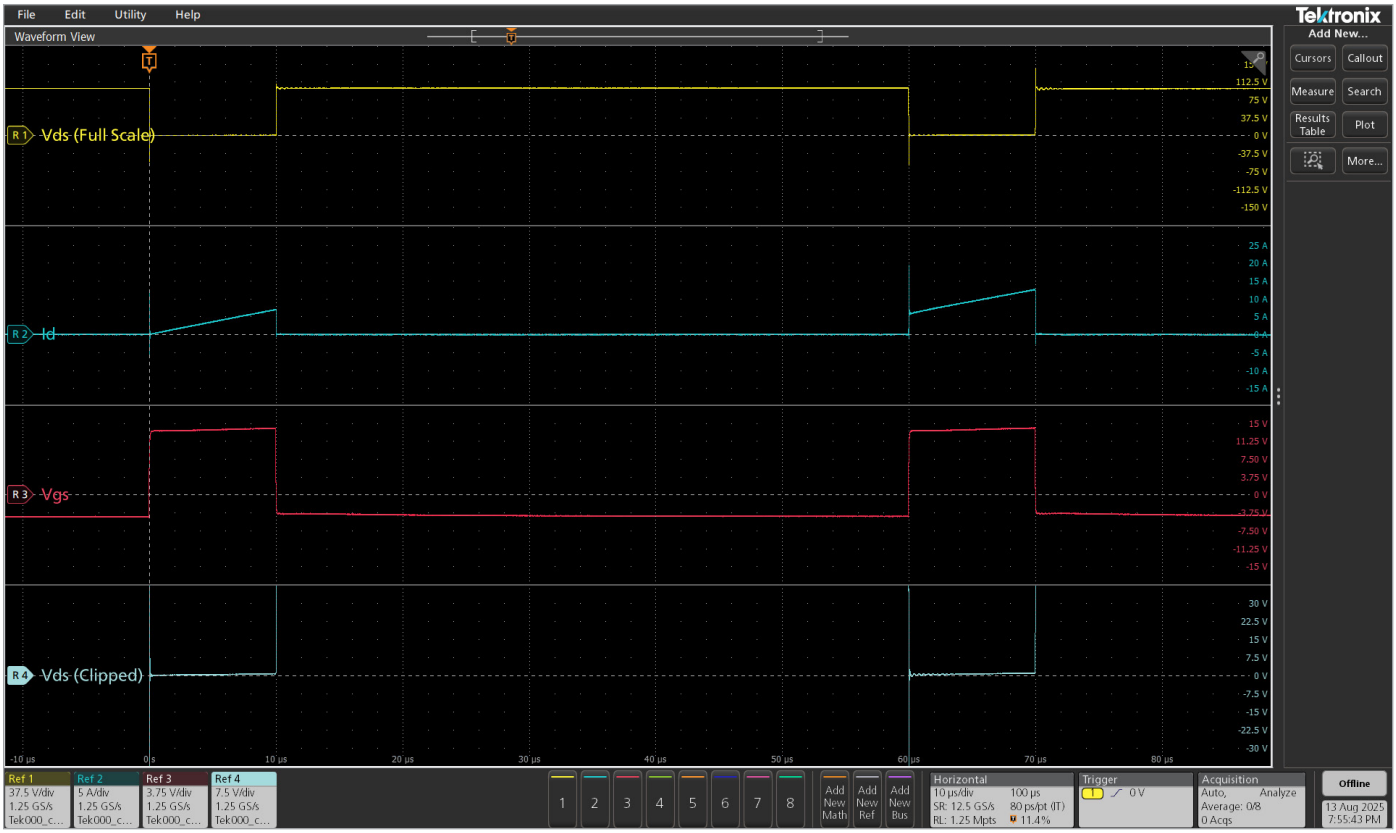


Figure 4. The Drain-Source Voltage (V_{DS}) is captured using a pair of THDP0200 High Voltage Differential Probes. One probe acquires the complete V_{DS} vertical data with an appropriate vertical scale. The other probe attached to V_{DS} acquires the data at a more sensitive vertical scale, which results in a clipping warning on the associated channel.

The WBG-DPT software combines the full-scale and high-sensitivity (but overdriven) V_{DS} waveforms to derive a high-resolution composite waveform for the drain-to-source voltage in the on state. Normally, overdriving a differential probe or the front end of an oscilloscope is not recommended, since measurements can be of questionable quality while the amplifier recovers from being driving beyond its rails. This is referred to as "overdrive recovery time" and is a common amplifier specification. The dynamic $R_{DS(on)}$ algorithm in the WBG-DPT application applies multiple techniques to mitigate the effects of:

- Excessive quantization ADC noise at low sensitivities (high V/div)
- Random noise
- Probe settling time, probe error and aberrations
- Overdrive recovery on clipped waveforms.

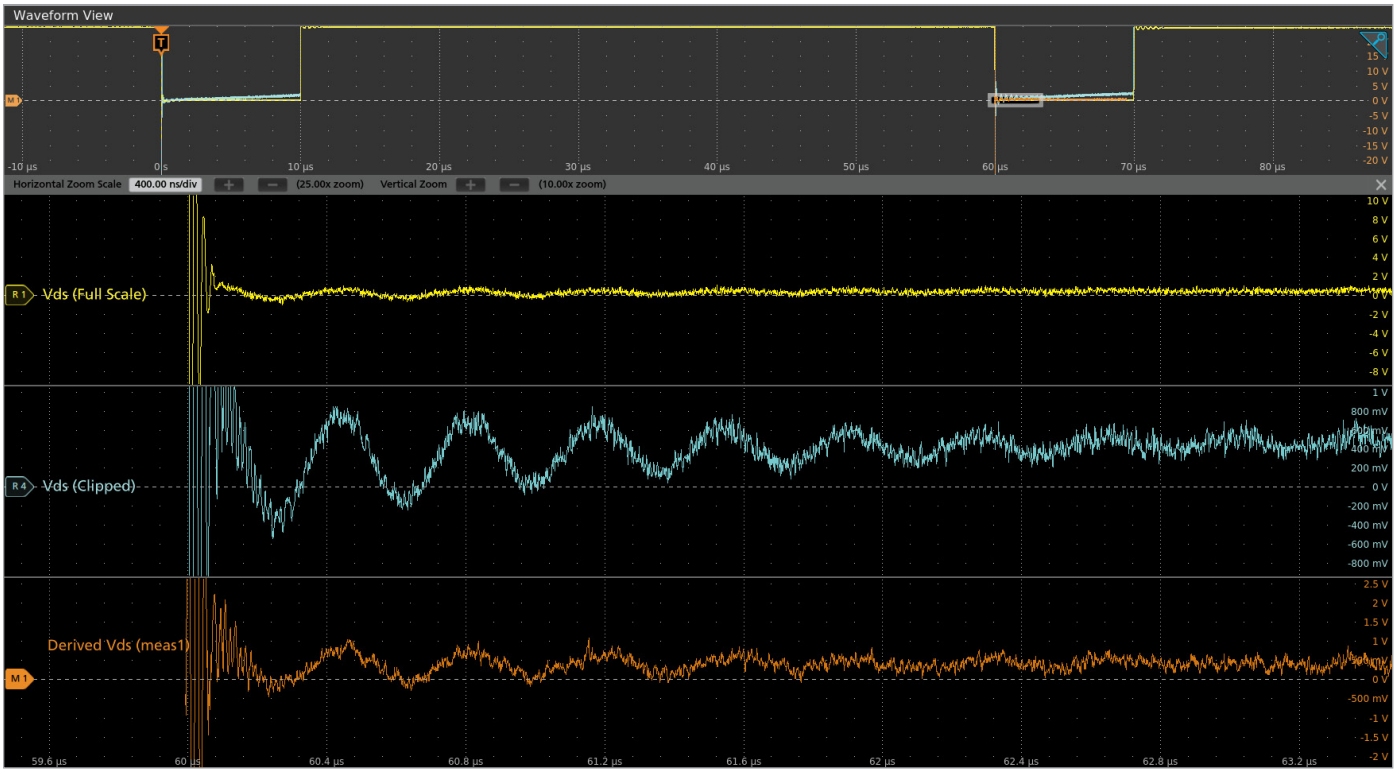


Figure 5. A clipped reference waveform (R4) and full-scale waveform (R1) are combined through signal processing to generate a derived $V_{DS(on)}$ (M1) which uses information from the full-scale V_{DS} to correct the clipped V_{DS} while maintaining the high-resolution information in the clipped waveform.

The effects of quantization error, settling time and overdrive recovery can be seen in **Figure 5**, Reference 4 which is overdriven/clipped shows extended ringing and a recovery time to reach actual voltage value. Reference 1 is unclipped, capturing the complete V_{DS} voltage signal up to the bus voltage, but with clear quantization issues.

Using Signal Conditioning to Derive Low-Noise $V_{DS(on)}$

In a typical Double Pulse Test (DPT), the switching device is initially turned on during the first pulse, allowing the current through the load inductor to increase linearly until it reaches the desired test level. The device is then turned off and subsequently reactivated with a second pulse to evaluate its switching performance at the specified test current. $R_{DS(on)}$ is measured during the second pulse.

The signal conditioning algorithm for $V_{DS(on)}$ assumes the following conditions are met:

- Two turn-on cycles are executed in bursts, as in a double pulse test. Information from the first pulse is used to enhance the second pulse. A 50 µs gap between first and second pulse is necessary so that any settling errors are the same for both turn-ons. Probes and oscilloscopes typically have time constants around 10 µs, so a 50 µs settling time is generally adequate.
- First and second pulse width should at least be 10 µs so that the algorithm can ignore the initial ripple and focus on the actual $R_{DS(on)}$.
- Sufficient delay between bursts exists to allow the DUT to stabilize between double pulse tests.
- The vertical scale of the clipped V_{DS} waveform is sensitive enough to provide adequate resolution, but not so sensitive that the signal is underrepresented.

The WBG-DPT application's PRESET function sets the scale automatically based on the specified V_{DS} switching voltage.

These steps outline the high-level steps within the Dynamic $R_{DS(on)}$ measurement algorithm.

1. Waveform averaging applied to multiple Double Pulse Tests

To reduce the impact of random noise on measurements, multiple double pulse tests may be performed and the resulting waveforms averaged. The WBG-DPT $R_{DS(on)}$ measurement provides a control for this and defaults to eight waveform averages per measurement.

2. Full-scale and Clipped $V_{DS(on)}$ segments are combined

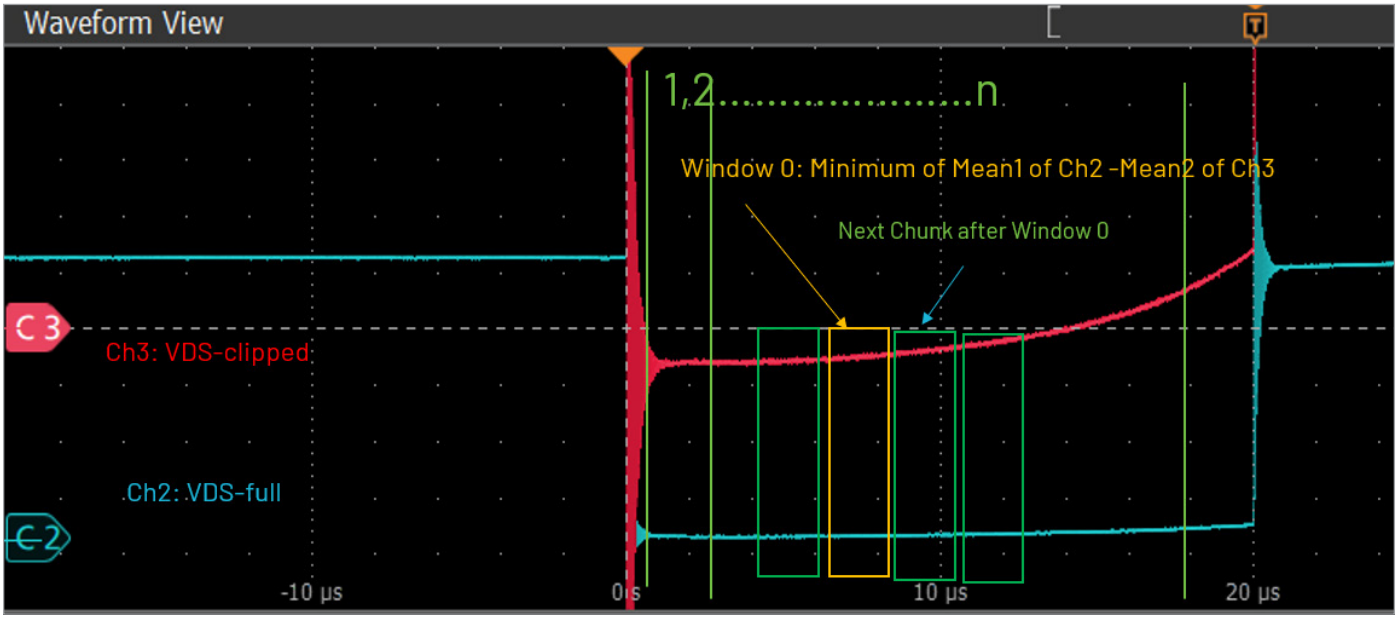


Figure 6. Combining full-scale (Channel 2) and clipped (Channel 3).

This process uses information from the full-scale $V_{DS(on)}$ and the clipped $V_{DS(on)}$ segments to construct a high-resolution, derived V_{DS} waveform.

- The algorithm divides the on-segments of both the full-scale, $V_{DS\text{-}full}$, and clipped, $V_{DS\text{-}clipped}$, samples into n horizontal windows each with k samples.
- Mean values, AVG($V_{DS\text{-}full}$) and AVG($V_{DS\text{-}clipped}$), of the samples are determined for each window.
- The window with the smallest difference between AVG($V_{DS\text{-}full}$) and AVG($V_{DS\text{-}clipped}$) is found. This window becomes the reference window, or Window 0. The average values here are AVG($V_{DS\text{-}full}$(0)) and AVG($V_{DS\text{-}clipped}$(0)).
- The difference between these two means is subtracted from all samples in the clipped V_{DS} window. This shifts the high-resolution $V_{DS\text{-}clipped}$ samples to the same average level as the full-scale $V_{DS\text{-}full}$ signal.
- The algorithm then moves on to the next window, for example Window 1. The difference between AVG($V_{DS\text{-}full}$(1)), and previous window, AVG($V_{DS\text{-}full}$(0), is found. Note that this difference represents the trend, up or down, of the full-scale signal. This difference is applied linearly to the $V_{DS\text{-}clipped}$ samples in Window 1 as a correction.
- This same "sliding window" process is applied to all windows before and after the reference window.

This correction maintains the high-resolution information in the clipped samples by using the unclipped full-scale signal to generate low-frequency offset corrections. A composite V_{DS} waveform with enhanced vertical resolution during the ON time is the result. The derived V_{DS} represents the ON region as though the time domain waveform had been acquired with lower vertical scale.

3. Turn-on 1 is subtracted from Turn-on 2 to remove settling errors

Within the composite V_{DS} waveform any settling errors in the two voltage steps between V_{DS}(off) and $V_{DS(on)}$ should be nearly identical in the first and second pulses, since the step size is approximately the same for both pulses. This assumes that the time between the two turn-ons is adequate to allow the measurement system to settle between cycles.

Thus, to remove consistent settling errors from the derived V_{DS}, samples from the first $V_{DS(on)}$ segment are subtracted from samples from the second $V_{DS(on)}$ segment. This removes both the settling error, as well as any $V_{DS(on)}$ common to both pulses. The remaining voltage in the second pulse will be due to the higher current flowing through $R_{DS(on)}$ in the second pulse. Id from the first on-cycle is subtracted from Id from the second cycle, to isolate the incremental current flowing through $R_{DS(on)}$.

Once the incremental voltage and current from the second off-cycle are known, the samples for $R_{DS(on)}$ are calculated using Ohm's Law. These samples are displayed and can be used to determine measurements such as average $R_{DS(on)}$ over the cycle. Note that due to the signal processing outlined above, only the $R_{DS(on)}$ associated with the second off-cycle is valid and displayed.

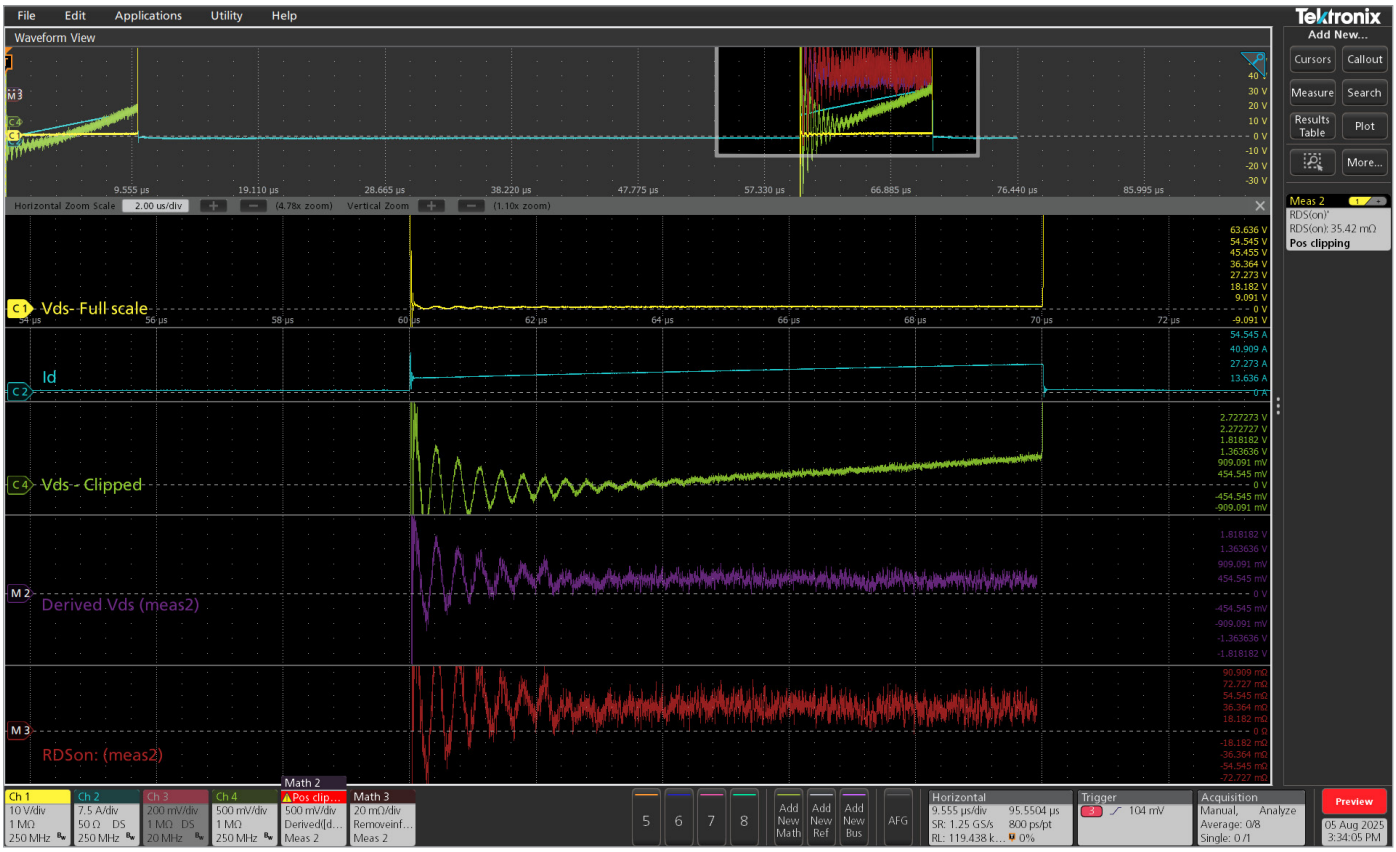


Figure 7. A 5 Series B MSO equipped with WBG-DPT Double Pulse Testing Analysis, measuring dynamic

Limitations on this New $R_{DS(on)}$ Measurement Technique

As with any procedure for measuring dynamic $R_{DS(on)}$, care must be taken when using this new method. As noted above, 10 µs pulse widths and a 50 µs gap between pulses are recommended. The clipped waveform has the restriction on the vertical scale. The algorithm has been tested using Tektronix THDP Series High Voltage Differential Probes but has not been tested using other probes. The method is not suitable for measuring dynamic $R_{DS(on)}$ of less than 10 mΩ.

Performing Dynamic $R_{DS(on)}$ Measurements Using Software Clamping Technique

Based on the theory of dynamic $R_{DS(on)}$ measurements and the double-probing technique outlined in the previous sections, we will now cover the application of the $R_{DS(on)}$ measurement using this new approach, including the test setup, procedure, and interpretation of results.

Test Setup

The test setup for performing dynamic $R_{DS(on)}$ measurements is shown in **Figure 8** and **Figure 9**.The system comprises:

- 4, 5 or 6 Series B MSO oscilloscope
- WBG-DPT Double Pulse Testing software license
- THDP0100 or THDP0200: 2 each for measuring clipped V_{DS} and full scale V_{DS} signals
- AFG 31000 Series function generator
- TRCP, TCP0030A or TCP0150 or CVR with TICP Current Probe or for measuring I_D
- TPP1000 for low side V_{GS}
- Power Supply to source V_{DD}
- SiC or GaN test board as DUT

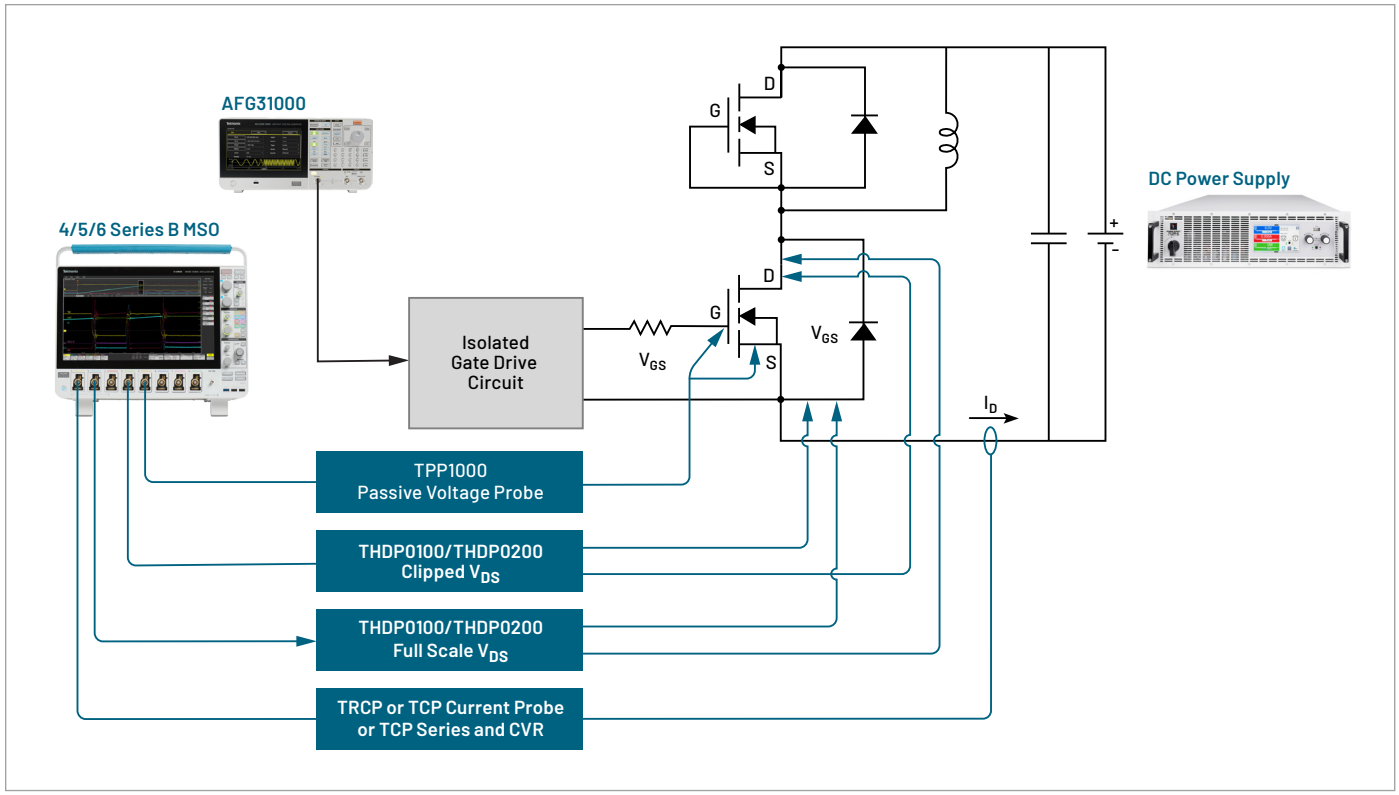


Figure 8. A test setup for measuring the dynamic $R_{DS(on)}$ of a low-side FET. Note that two high-voltage differential probes are applied across the drain and source terminals of the FET.

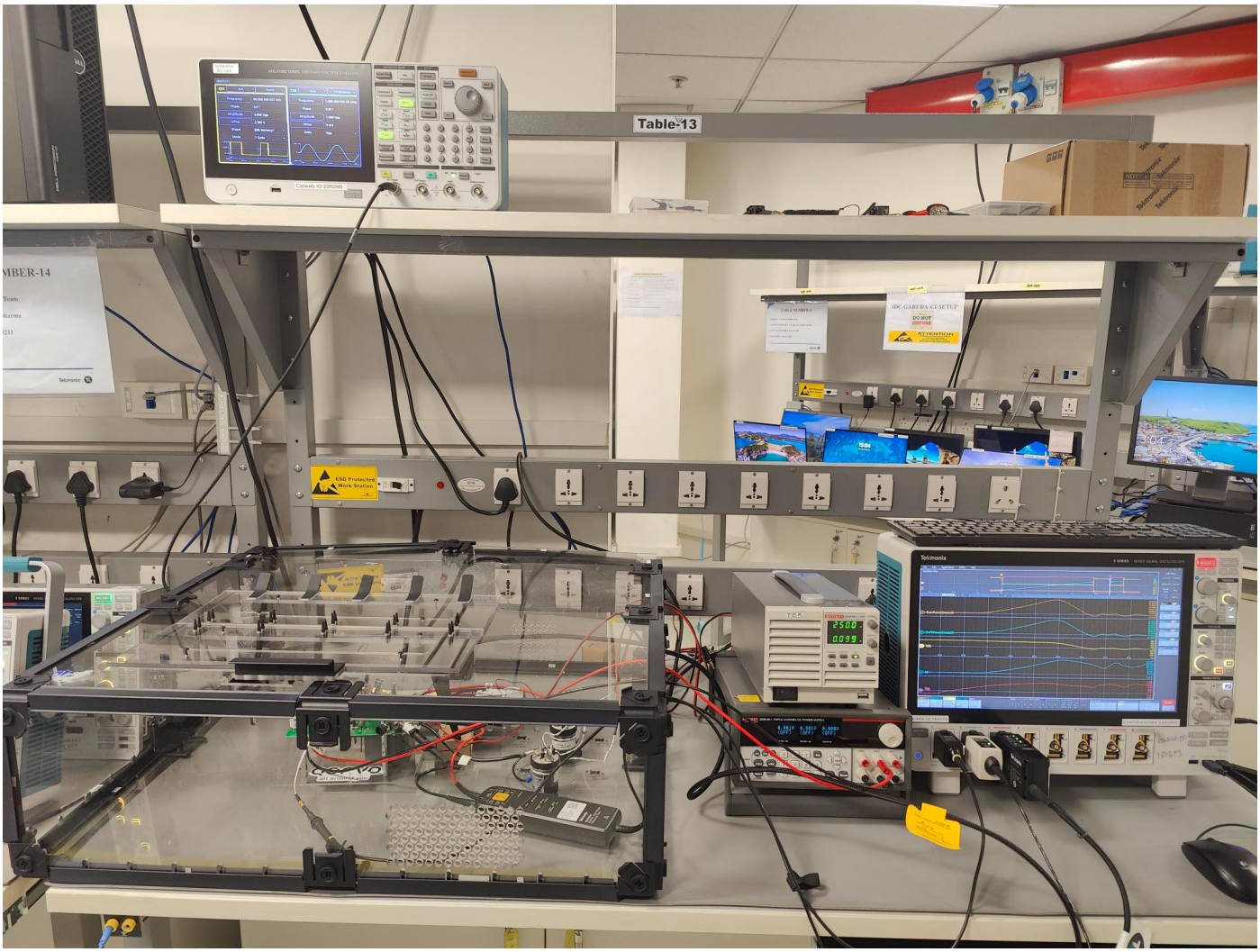


Figure 9. Dynamic $R_{DS(on)}$ test setup in a lab.

Dynamic $R_{DS(on)}$ Measurement Steps

On the oscilloscope, the $R_{DS(on)}$ measurement is added from the WBG-DPT Add Measurements Panel (**Figure 10**). The settings for the dynamic $R_{DS(on)}$ measurement are opened by double-clicking on the measurement badge. This opens the panel shown in **Figure 11**. The five steps for setting up the measurement are shown in the panel.

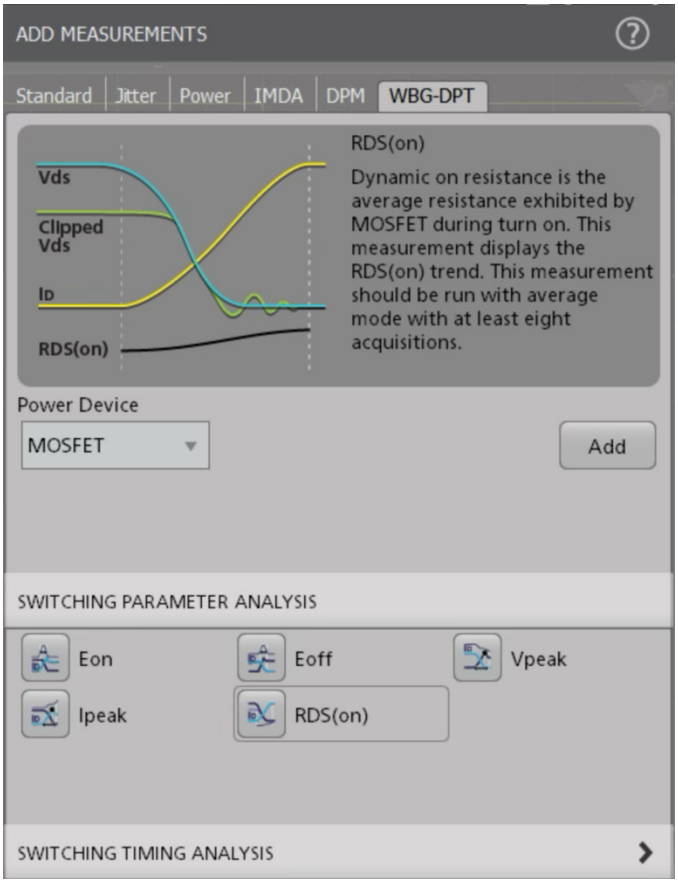


Figure 10. In the WBG-DPT application, the $R_{DS(on)}$ measurement is one of several switching parameter measurements.

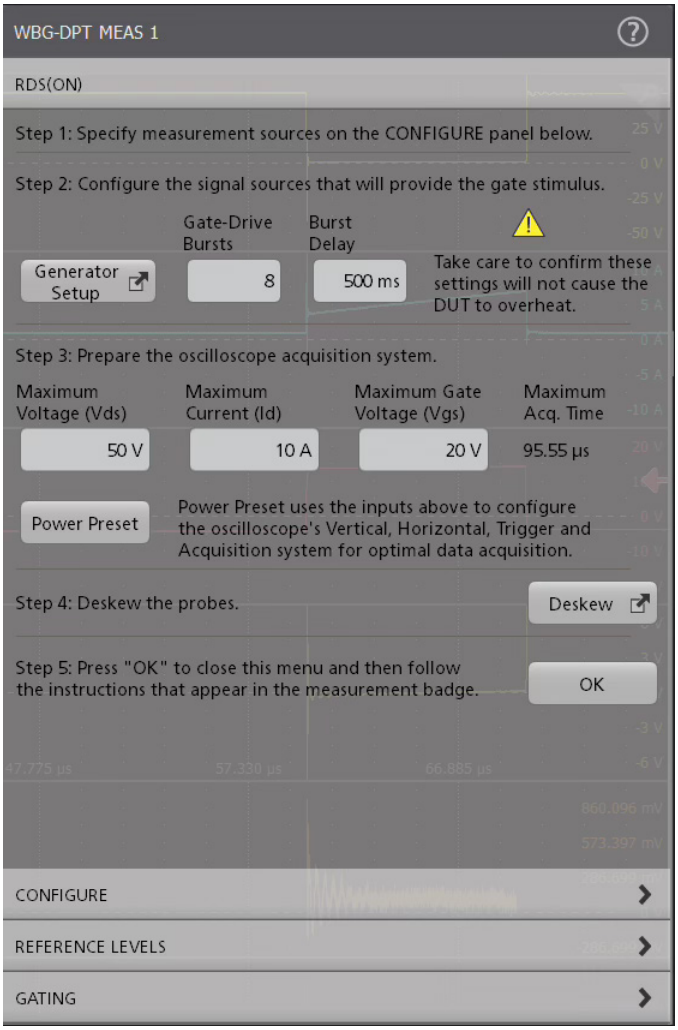


Figure 11. The $R_{DS(on)}$ measurement panel outlines the steps for making the measurement.

1. First, the Configure panel is opened and the channel assignments for Vds full scale, Vds clipped, Id and Vgs are made.

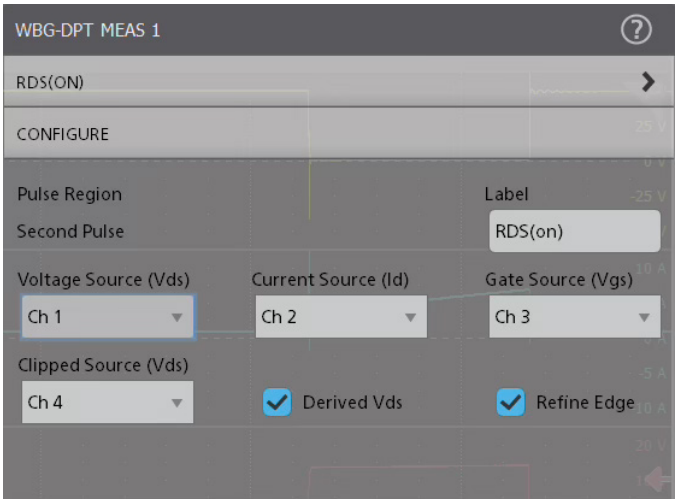


Figure 12. Assigning oscilloscope input channels to voltage and current sources.

2. Next, the LAN-connected AFG31000 is configured to generate the double pulse test signal.The first and second pulses should at least be 10 µs wide with a 50 µs gap between first and second pulse, as explained in "Signal Conditioning to Derive Low-Noise $V_{DS(on)}$", above.

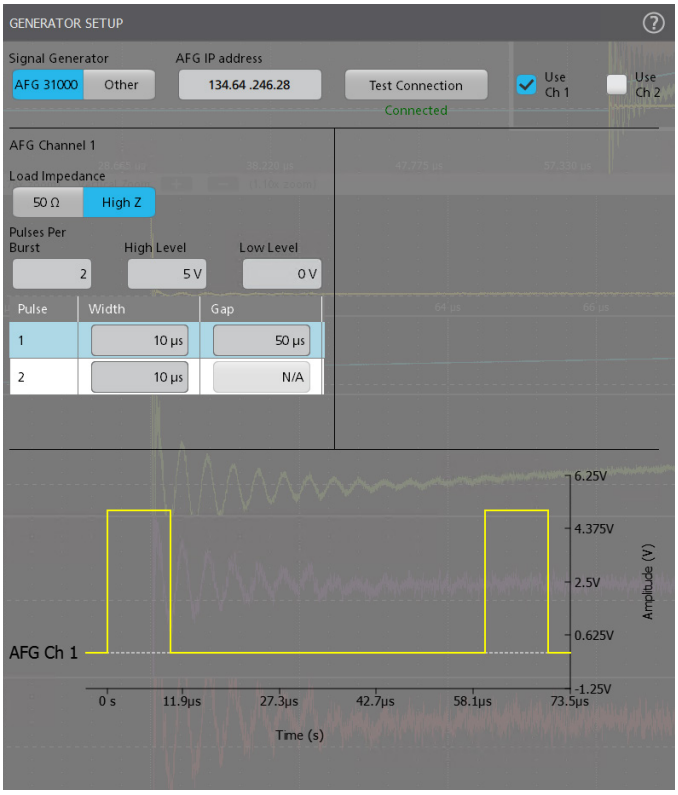


Figure 13. Setting up the double pulse stimulus from the signal generator, with 10 µs pulses separated by a 50 µs gap.

3. The nominal maximum values of Vds, Id and Vgs are entered.Clicking on Power Preset uses this information to configure the oscilloscope's vertical scales, horizontal scale, trigger and acquisition settings.

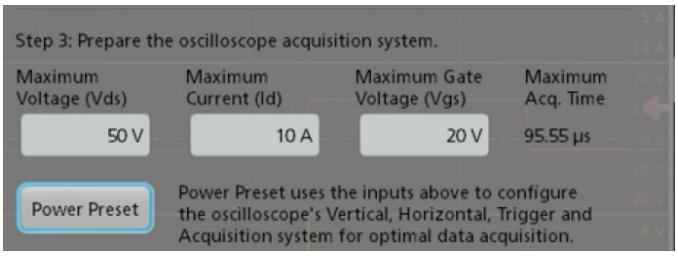


Figure 14. Nominal maximums are used to set scaling.

4. The current and voltage probes are deskewed using the special software deskew process built into the WBG-DPT software. Clicking on the WBG Deskew button acquires voltage and current waveforms, and automatically adjust channel-to-channel delay to compensate for different probe delays.

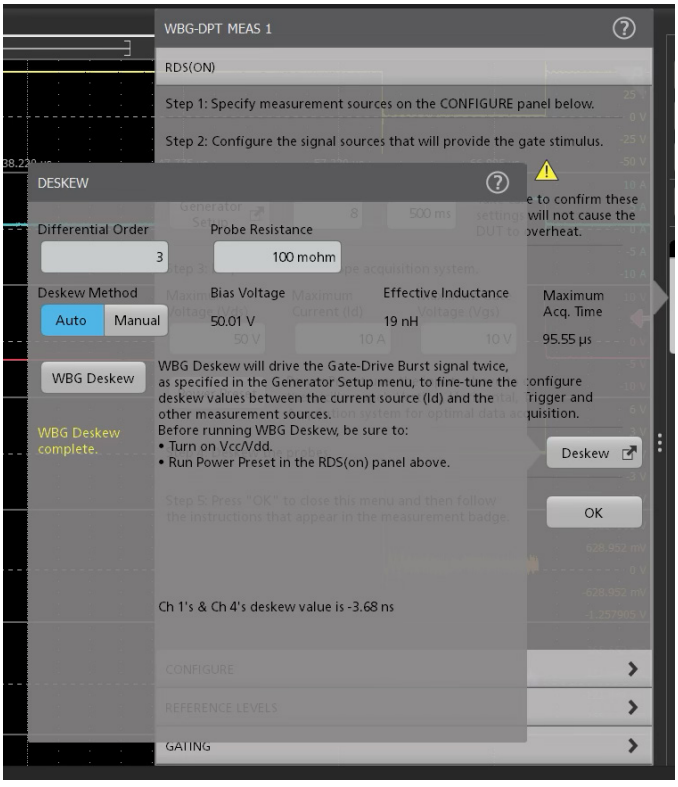


Figure 15. WBG Deskew is used to automatically remove timing skew between probes.

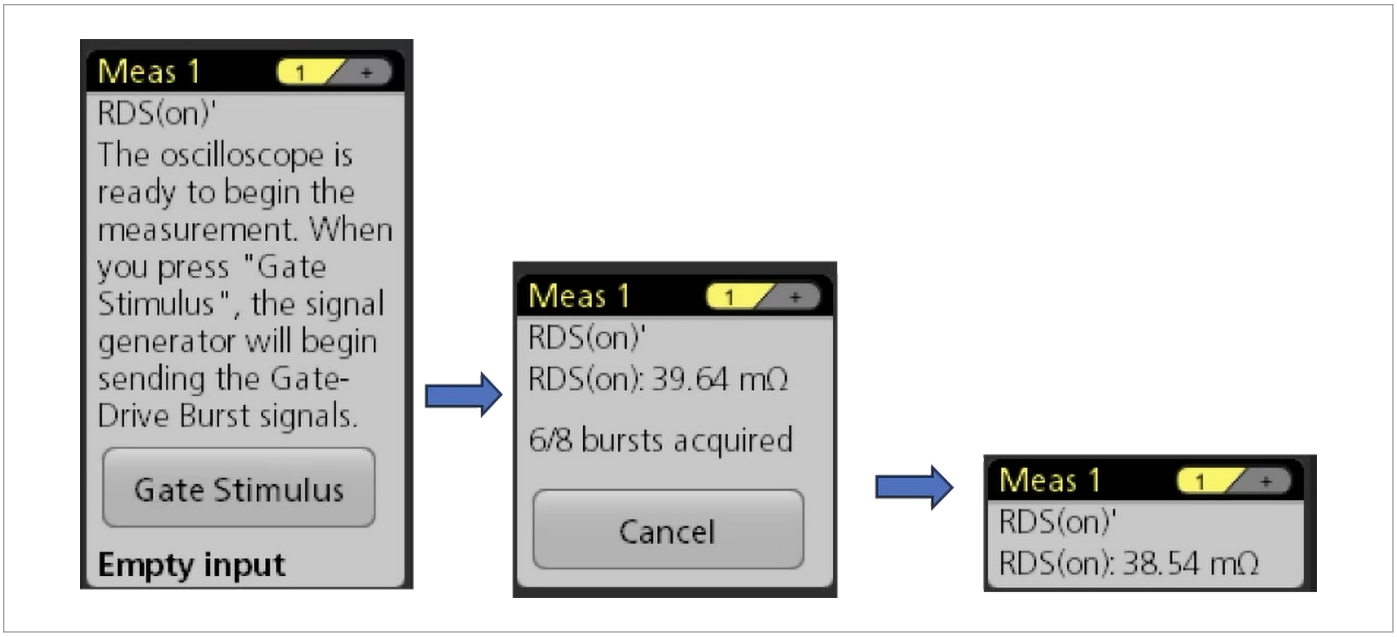


Figure 16. After clicking OK in the $R_{DS(on)}$ panel the oscilloscope is ready to acquire waveforms. The measurement badge now includes a button to initiate the Gate Stimulus. During the test it shows the number of complete acquisitions and after the test it shows the number of completed acquisitions and after the test it sows the average dynamic $R_{DS(on)}$.

5. The OK button in the $R_{DS(on)}$ panel is clicked and the oscilloscope is ready to make the measurement. A Gate Stimulus button appears in the measurement badge, as shown in **Figure 16**. Once this button is clicked, the measurement badge shows the number of completed acquisitions, followed by the final average $R_{DS(on)}$.

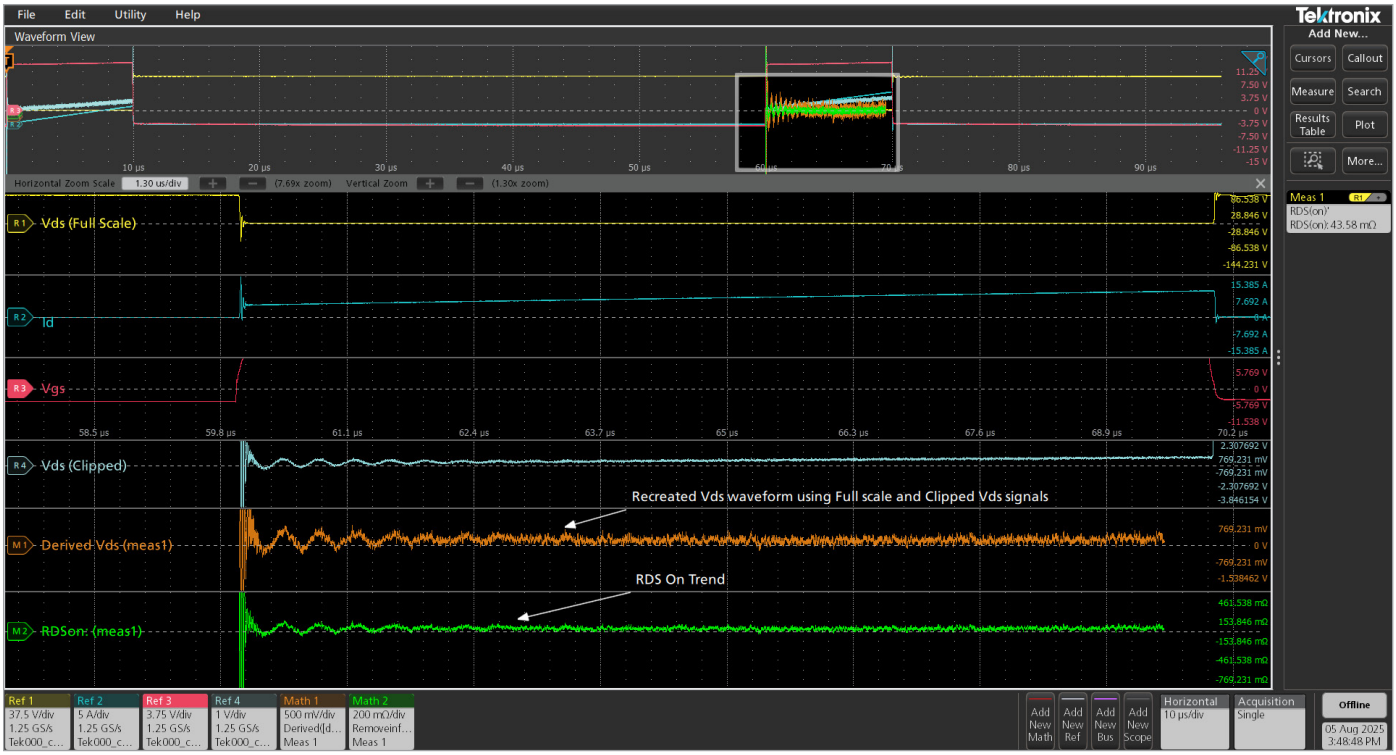


Figure 17. An $R_{DS(on)}$ measurement result on the 5 Series B MSO.

Measurement Results

As shown in **Figure 17**, after initiating the $R_{DS(on)}$ measurement from the measurement panel, the oscilloscope will acquire the V_{DS} (clipped and un-clipped) and I_D signals. The $R_{DS(on)}$ measurement algorithm uses the two V_{DS} signals to calculate a high-resolution, composite V_{DS} signal during the second turn-on stage. This is shown in **Figure 18**.The composite V_{DS} signal is divided by I_D to find $R_{DS(on)}$ during the second turn on stage.

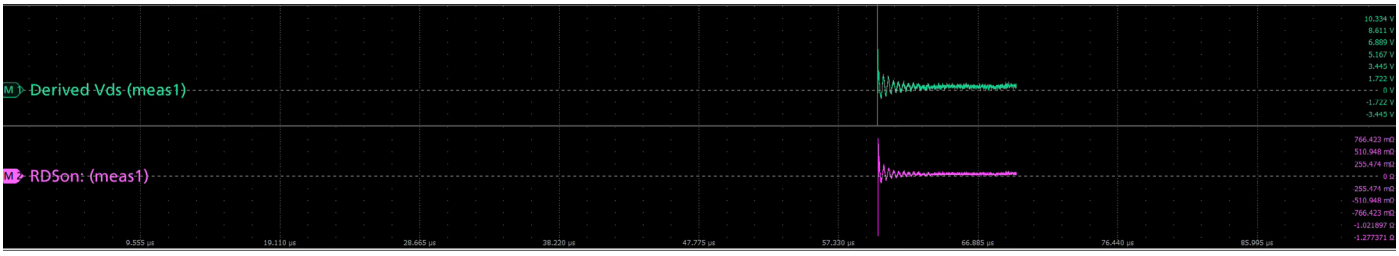


Figure 18. Derived V_{DS} and $R_{DS(on)}$ waveform detail from the $R_{DS(on)}$ measurement.

The software method has been shown to correlate well with clamping circuits. While there will be variations between individual power devices, this method has been shown to provide a general indication of how $R_{DS(on)}$ changes with current and temperature. An example set of results for the software method and traditional hardware clamping is shown in **Figure 19** for comparison.

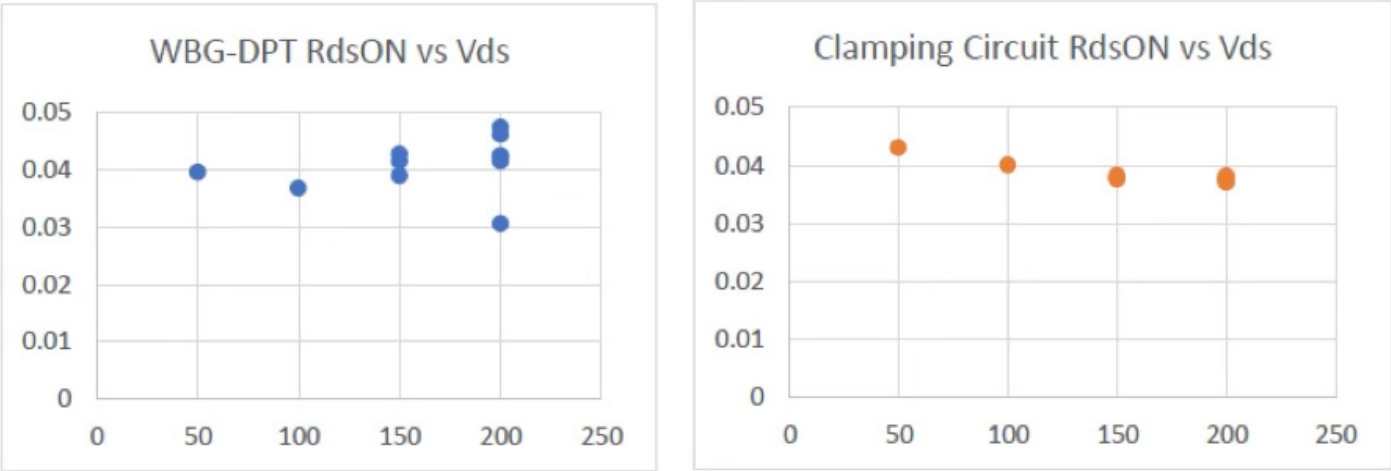


Figure 19. Scatter plot of the $R_{DS(on)}$ measurement of a Qorvo MOSFET, using the software clamping method (left) and an external clamping circuit (right).

Conclusion

This oscilloscope-based clamping approach can provide a way to compare measured results to expected results. It should not be used for device characterization, but can guide designers as they evaluate devices and designs. This signal-processing approach provides useful measurements of dynamic $R_{DS(on)}$ in WBG devices, facilitating better optimization of switching efficiency and thermal management strategies. This method simplifies the test setup while providing an accurate representation of device behavior under high frequency switching conditions.

References

1. L. Ren, Q. Shen and C. Gong, "A voltage clamp circuit for the real-time measurement of the on-state voltage of power transistors," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016, pp. 1-7, doi: 10.1109/ECCE.2016.7854807. A voltage clamp circuit for the real-time measurement of the on-state voltage of power transistors | IEEE Conference Publication | IEEE Xplore
2. M. Šír and I. Feňo, "Measurement Method for the Dynamic On-State Resistance of GaN Semiconductors," 2018 2nd European Conference on Electrical Engineering and Computer Science (EECS), Bern, Switzerland, 2018, pp. 543-546, doi: 10.1109/EECS.2018.00106. https://ieeexplore.ieee.org/document/8910040
3. A. N. Rahman, M. -Y. Li, M. Tampubolon and H. -J. Chiu, "High Resolution Dynamic $R_{DS(on)}$ Measurement of GaNFET using Active $V_{DS(on)}$ Measurement Clamp Circuit," 2019 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Taipei, Taiwan, 2019, pp. 1-4, doi: 10.1109/WiPDAAsia.2019.8760329. High Resolution Dynamic RDS(on) Measurement of GaNFET using Active VDS(on) Measurement Clamp Circuit | IEEE Conference Publication | IEEE Xplore

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Rev. 02.2022

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082225 48W-74181-0